**Chapter 14 - Exercises**

14.1. What general roles are performed by processor registers?

**The general roles performed by processor registers are mainly from two registers; the User-visible register and the Control & status registers.**

**User-visible registers: These enable the machine- or assembly language programmer to minimize main-memory references by optimizing use of registers.**

**Control and status registers: These are used by the control unit to control the operation of the CPU and by privileged, operating system programs to control the execution of programs.**

14.2. What categories of data are commonly supported by user-visible registers?

**The categories of data supported by user-visible registers are:**

**1. General purpose**

**2. Data**

**3. Address**

**4. Condition codes**

14.3. What is the function of condition codes?

**Condition codes are bits set by the CPU hardware as the result of operations. For example, an arithmetic operation may produce a positive, negative, zero, or overflow result. In addition to the result itself being stored in a register or memory, a condition code is also set. The code may subsequently be tested as part of a conditional branch operation.**

14.4. What is a program status word?

**All CPU designs include a register or set of registers, often known as the program status word (PSW), that contain status information. The program status word typically contains condition codes plus other status information.**

14.5. Why is a two-stage instruction pipeline unlikely to cut the instruction cycle time in half, compared with the use of no pipeline?

**Here's why a two-stage instruction pipeline is unlikely to cut the instruction cycle time in half, compared with the use of no pipeline;**

**The execution time will generally be longer than the fetch time. Execution will involve reading and storing operands and the performance of some operation. Thus, the fetch stage may have to wait for some time before it can empty its buffer.**

**A conditional branch instruction makes the address of the next instruction to be fetched unknown. Thus, the fetch stage must wait until it receives the next instruction address from the execute stage. The execute stage may then have to wait while the next instruction is fetched.**

14.6. List and briefly explain various ways in which an instruction pipeline can deal with conditional branch instructions.

**Below are some of the ways in which an instruction pipeline can deal with conditional branch instructions;**

**Multiple streams: A brute-force approach is to replicate the initial portions of the pipeline and allow the pipeline to fetch both instructions, making use of two streams.**

**Prefetch branch target: When a conditional branch is recognized, the target of the branch is prefetched, in addition to the instruction following the branch. This target is then saved until the branch instruction is executed. If the branch is taken, the target has already been prefetched.**

**Loop buffer: A loop buffer is a small, very-high-speed memory maintained by the instruction fetch stage of the pipeline and containing the n most recently fetched instructions, in sequence. If a branch is to be taken, the hardware first checks whether the branch target is within the buffer. If so, the next instruction is fetched from the buffer.**

**Branch prediction: A prediction is made whether a conditional branch will be taken when executed, and subsequent instructions are fetched accordingly.**

**Delayed branch: It is possible to improve pipeline performance by automatically rearranging instructions within a program, so that branch instructions occur later than actually desired.**

14.7. How are history bits used for branch prediction?

**One or more bits that reflect the recent history of the instruction (history bits) can be associated with each conditional branch instruction. These bits are referred to as a taken/not taken switch that directs the processor to make a particular decision the next time the instruction is encountered.**

14.8. What would be the value of the following flags: Carry, Zero, Overflow, Sign, Even Parity , Half-Carry ?

(a) If the last operation performed on a computer with an 8-bit word was an addition in which the two operands were 00000010 and 00000011.

(b) Repeat for the addition of -1 (twos complement) and +1.

(c) A - B, where A contains 11110000 and B contains 0010100.

**Answers to Questions**